What is claimed is:

1. A semiconductor package comprising:

a first die pad and a plurality of leads arranged about the periphery of the first die pad wherein the first die pad and the leads have a thickness between about 10 mils and about 20 mils;

a first semiconductor device securely attached to an upper surface of the first die pad; the first semiconductor device being electrically coupled to one of the leads; and

a package body formed over the semiconductor device and the leads in a manner that the lower surfaces of the first die pad and the leads are exposed through the package body.

2. The semiconductor package as claimed in claim 1, wherein the first semiconductor device is a power semiconductor device and the power semiconductor device is securely attached to the upper surface of the first die pad by solder paste.

3. The semiconductor package as claimed in claim 1, further comprising an output bar wherein the first semiconductor device is electrically coupled to the output bar by at least one heavy gauge aluminum wire.

4. The semiconductor package as claimed in claim 1, further comprising a second die pad having a thickness between about 10 mils and about 20 mils and disposed between the leads, and a second semiconductor device which is securely attached to the second die pad and electrically coupled to the leads and the first semiconductor device by a plurality of gold wires.

5. The semiconductor package as claimed in claim 4, wherein the second semiconductor device is a control semiconductor device.

6. The semiconductor package as claimed in claim 4, wherein the second semiconductor device is a control semiconductor device and the control semiconductor device is securely attached to the second die pad by silver epoxy.

7. The semiconductor package as claimed in claim 1, wherein each lead and the die pad are half-etched to form indentations thereby significantly enhancing the locking of the leads and the die pad in the package body.

8. A semiconductor package comprising:

first and second die pads, and an output bar and a plurality of leads arranged about the periphery of the first and second die pads wherein the first and second die pads;

a first semiconductor device securely attached to the first die pad, the first semiconductor device being electrically coupled to the output bar by at least one heavy gauge aluminum wire;

a second semiconductor device securely attached to the second die pad, the second semiconductor device being electrically coupled to the leads and the first semiconductor device; and

a package body formed over the first semiconductor device, the second semiconductor device, the output bar and the leads in a manner that the lower surfaces of the output bar and the leads are exposed through the package body.

9. The semiconductor package as claimed in claim 8, wherein:

the first semiconductor device is a power semiconductor device and the power semiconductor device is securely attached to the upper surface of the first die pad by solder paste, and

the second semiconductor device is a control semiconductor device and the control semiconductor device is securely attached to the second die pad by silver epoxy.

10. The semiconductor package as claimed in claim 8, wherein each lead and the die pads are half-etched to form indentations thereby significantly enhancing the locking of the leads and the die pads in the package body.

11. A semiconductor package comprising:

first and second die pads, and a plurality of leads arranged about the periphery of the first and second die pads wherein the die pads and the leads have a thickness between about 10 mils and about 20 mils;

a first semiconductor device securely attached to the first die pad;

a second semiconductor device securely attached to the second die pad, the second semiconductor device being electrically coupled to the leads and the first semiconductor device; and

a package body formed over the first semiconductor device, the second semiconductor device, and the leads in a manner that the lower surfaces of the leads are exposed through the package body.

12. The semiconductor package as claimed in claim 11, wherein:

the first semiconductor device is a power semiconductor device and the power semiconductor device is securely attached to the upper surface of the first die pad by solder paste, and

the second semiconductor device is a control semiconductor device and the control semiconductor device is securely attached to the second die pad by silver epoxy.

13. The semiconductor package as claimed in claim 11, wherein each lead and the die pads are half-etched to form indentations thereby significantly enhancing the locking of the leads and the die pads in the package body.

14. A process for making a plurality of semiconductor packages, comprising the following steps:

providing a lead frame having a thickness between about 10 and about 20 mils, the lead frame including a plurality of units in an array arrangement, each unit having first and second die pads, and an output bar and a plurality of leads arranged at the periphery of the die pads, each lead having an half-etched indentation formed corresponding to a predetermined dicing line;

attaching a first semiconductor device onto the first die pad of each unit of the lead frame by solder paste;

attaching a second semiconductor device onto the second die pad of each unit of the lead frame by silver epoxy;

electrically coupling the first semiconductor device to the output bar;

electrically coupling the second semiconductor device to the leads and the first semiconductor device;

forming a molded product by encapsulating the semiconductor devices against the lead frame to form a plurality of package bodies each encapsulating the first semiconductor device and the second semiconductor device; and

cutting the molded product along the half-etched indentations of the leads into individual semiconductor packages.

15. The process as claimed in claim 14, wherein the first semiconductor device is electrically coupled to the output bar by at least one heavy gauge aluminum wire.

16. The process as claimed in claim 14, wherein the second semiconductor device is electrically coupled to the leads and the first semiconductor device by a plurality of gold wires.

17. The process as claimed in claim 14, wherein the first semiconductor device is a power semiconductor device and the second semiconductor device is a control semiconductor device.

18. The process as claimed in claim 14, wherein the cutting step comprises a step of sawing the molded product into individual semiconductor packages.

19. The process as claimed in claim 14, wherein the molded product has opposing upper and lower surfaces, one surfaces of the die pads and the leads are exposed from the lower surface of the molded product and the cutting step comprises a step of sawing the molded product into individual semiconductor packages from the lower surface of the molded product to the upper surface of the molded product.

20. The process as claimed in claim 14, wherein the cutting step comprises a step of punching the molded product into individual semiconductor packages.